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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/825,616	04/16/2004	Yong Ho Jang	8734.298	7873

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EXAMINER	
TSEGAYE, DANIEL	

ART UNIT	PAPER NUMBER
2629	

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09/28/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/825,616	JANG ET AL.	
	Examiner	Art Unit	
	DANIEL TSEGAYE	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 August 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,13,14,16 and 23-25* is/are rejected.

7)☒ Claim(s) *10-12,15 and 17-22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. *The amendment filed on 06/28/2007 has been entered and considered by the examiner.*

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-9,13-14,16,22-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishii (U.S P# 6,670,944) in view of Park (U.S Pub# 2004/0109526), further in view of Kanzaki (U.S Pat # 6,967,639).

As to claim 1, Ishii discloses a gate driving apparatus for a liquid crystal display, comprising: a shift register (1560) provided with first (e.g., CLX) and second half-period clock signals (e.g., CLX_{INV}) phases inverted with respect to each other (see Fig. 13), a start pulse (e.g., DX), a high-level supply voltage (e.g., VGG) and a low-level supply voltage (e.g., VSS). Ishii does not teach first to fourth one-period clock signals having phases shifted sequentially and each having a pulse width of one period. Park teaches first to fourth one-period clock signals having phases shifted sequentially and each having a pulse width of one period (see Fig. 10 and [0119]).

Therefore, it would have obvious to one of ordinary skill in the art at time the invention was made to have provided with first to fourth one-period clock signals having

phases shifted sequentially and each having a pulse width of one period as taught by park to the elect optical device of Ishii because the thin transistor in the shift register of Park minimize the level of voltage in while reducing power dissipation (see [0023]).

Ishii and Park do not teaches wherein the shift register generates a half-period output, and generates a one-period output at a half-period delay from an end time of the half-period output. Kanzaki teaches wherein the shift register generates a half-period output, and generates a one-period output at a half-period delay from an end time of the half-period output (see col. 6, lines 42-48).

Therefore, it would have obvious to one of ordinary skill in the art at time the invention was made to have provided with shift register generates a half-period output, and generates a one-period output at a half-period delay from an end time of the half-period output as taught by Kanzaki to the shift register of Ishii as modified by Park because it is possible to drive a display device having a multiplex pixel structure only with simple on or off signal and simplify the structure of a scan line drive circuit (see col.16 lines 66-67 and col. 17, lines 1-2).

As to claim 22, this claim differs from 1 only in that claim 1 is apparatus whereas claim 22 is method.

As to claim 4, this claim differs from 1 only in the limitations "first input circuit for charging a first charge control node" and "for charging a first discharge control node" are additionally recited. Park clearly teaches first input circuit (e.g., T1r and T2r) for charging a first charge control node (e.g., Q) and for charging a first discharge control node (e.g., QB, see [0089]).

As to claim 24, this claim differs from 4 only in that claim 4 is apparatus whereas claim 24 is method. In addition, claim 24 differs from 4 only the limitation "charging the second charge control node" and "charging the second discharge control node" are additionally recited. Park clearly teaches charging the second charge control node (e.g., QL, see [0162]), charging the second discharge control node (see Fig. 6, e.g., the node between T10r and T11r) also (see [0026]).

As to claim 2, Park teaches wherein the stages are connected in a cascade arrangement (see [0014]).

As to claims 3 and 23, Ishii teaches wherein any of the first (e.g., CLX) and second half-period clock signals (e.g., CLX_{INV}), any one of the first to fourth one-period clock signals (e.g., C2) and the start pulse are synchronized with each other (see Fig. 13).

As to claim 5, note the discussion of Ishii and Park above in claim 24.

As to claim 6, Park teaches wherein the first input circuit (e.g., T1r and T2r), the first output circuit (e.g., T6r), the second input circuit and the second output circuit are included in each of a plurality of stages (see [0025]).

As to claim 7, Park teaches wherein the start pulse is applied to first stage of the plurality of stages (see [0026]).

As to claim 8, Ishii teaches wherein the first half-period clock signal (e.g., CLX_{INV}) is synchronized with the second clock signal (e.g., CLX) and start pulse (e.g., DX) are synchronized with each other (see Fig. 13).

As to claim 9, Park teaches wherein the first input circuit (e.g., T1r and T2r) for charging the first charge control node (e.g., Q) (see Fig. 6). Ishii teaches an inverter (1590) and also the limitation a half-period delay from the end time of the start pulse in response to the start pulse (e.g., DX) and the first half-period clock signal (e.g., C1) (see Fig. 11).

As to claim 13, Park teaches a sixth transistor (e.g., T4r) having a gate electrode supplied with first clock signal (e.g., C3) and a source electrode supplied with a high-level supply voltage (e.g., VDD); and

A seventh transistor having a gate electrode supplied with the first half-period clock signal (e.g., SP), a source electrode connected to a drain electrode of the sixth transistor, and drain electrode connected to the first discharge control node (e.g., QL) (see Fig.6).

As to claim 14, Park teaches an eighth transistor (e.g., T13r) having a gate electrode supplied with start pulse (e.g., Sp), a drain electrode supplied with a low-level supply voltage (e.g., VSS), and a source electrode connected to the first discharge control node (e.g., QL); and

A ninth transistor (e.g., T8r) having a drain electrode supplied with a low-level supply voltage (e.g., VSS), a gate electrode connected to the output node (e.g., LO1) and a source electrode connected to the first discharge control node (e.g., QL) (see Fig.6).

As to claim 16, this claim differs from 9 only the limitation "an inverter for charging the second charge control node". Park teaches an inverter (e.g., T10r) for charging the second charge control node (e.g., QL) (see [0084])

As to claim 25,Ishii teaches wherein the first half-period clock signal (e.g., CLX), the second clock signal (e.g., CLX_{INV}) and the start pulse (DX) are synchronized with each other (see Fig.13).

Allowable Subject Matter

4. Claims 10-12, 15,17-21 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

5. Applicant's arguments filed 06/28/2007 have been fully considered but they are not persuasive.

On page 10 last paragraph, claims 1-9, 13-14, 16 and 22-25, the Applicant argues that the cited references, singly or in combination does not teaches or suggest at least this feature of the claimed invention. The reference Ishii, Park and Kanzaki combined meets the limitation of claimed invention.

On page 11, second paragraph claim 4, the Applicant argues that the cited references, singly or in combination does not teaches or suggest at least this feature of the claimed invention. The reference of Ishii teaches first and second half-period clock signals phases inverted with respect to each other. Park teaches first to fourth one-period clock signals having phases shifted sequentially and each having a pulse width

of one period and Kanzaki teaches the shift register generates a half-period output, and generates a one-period output at a half-period delay from an end time of the half-period output as addressed in the office action. Thus, combining Ishii, Park and Kanzaki meets the limitation of claimed invention.

On page 11, fourth paragraph claim 22, the Applicant argues that the cited references, singly or in combination does not teaches or suggest at least this feature of the claimed invention. The reference of Ishii teaches first and second half-period clock signals phases inverted with respect to each other and a high-level supply voltage and a low-level supply voltage. Park teaches first to fourth one-period clock signals having phases shifted sequentially and each having a pulse width of one period and Kanzaki teaches the shift register generates a half-period output, and generates a one-period output at a half-period delay from an end time of the half-period output, combined meets the limitation of claimed invention.

On page 12, second paragraph claim 24, the Applicant argues that the cited references, singly or in combination does not teaches or suggest at least this feature of the claimed invention. The reference Ishii teaches first and second half-period clock signals phases inverted with respect to each other, Park teaches first to fourth one-period clock signals having phases shifted sequentially and each having a pulse width of one period clearly teaches charging the second charge control node (e.g., QL, see [0162]), charging the second discharge control node (see Fig. 6, e.g., the node between T10r and T11r) also (see [0026]).

Conclusion

6. Applicant's arguments filed 08/23/2007 have been fully considered but they are not persuasive. Accordingly, **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DANIEL TSEGAYE whose telephone number is 571 270-1715. The examiner can normally be reached on Monday-Friday, 8:005:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, CHANH NGUYEN can be reached on 571 272 7772. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Daniel Tsegaye
Sept 18, 2007

CHANH D. NGUYEN
SUPERVISORY PATENT EXAMINER